

09/515158

COFC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

October 11, 2005

Patent Number: 6,950,816 ^{B1}
Issued: September 27, 2005
Title: Built in Headroom for a
Preemptive Multitasking
Operating System Sizer
Our File: RA 5247K (1028.1126101)

Name of Patentees: John M. Quernemoen
Mark G. Hazzard

Customer No.: 27516

Attn: Certificate of Correction Branch
Commissioner for Patents
P O Box 1450
Alexandra, VA 22313-1450


Certificate
OCT 19 2005
of Correction

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR PTO MISTAKE (37 C.F.R. § 1.322(a))

1. Enclosed, in duplicate, is PTO/SB/44 (also Form PTO-1050), with at least one copy being suitable for printing.
2. In column 17, line 12 following the term "includes" the term "an" should be inserted. Enclosed for your ease of reference is a copy of page 3 of the Amendment filed on October 13, 2004, where the wording is shown correctly in claim 10. Due to canceling of some claims in the Amendment, the issued claim number is now claim 3 in U.S. Patent No. 6,950,816. Applicant respectfully requests the error be corrected.
3. Please send the Certificate to:

Name: Unisys Corporation
Charles A. Johnson
Address: P O Box 64942
MS 4773
St. Paul, MN 55164

Unisys Corporation
(type or print name of assignee)


Signature of person authorized to
sign on behalf of assignee

- ☒ Assignment recorded on February 29, 2000

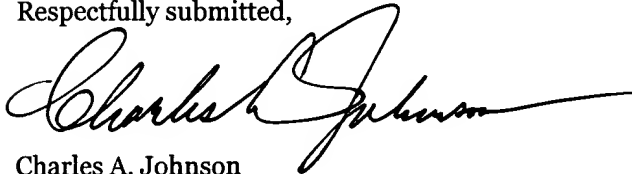
Reel 010654
Frame 0161

Charles A. Johnson
(type or print name of authorized person signing)
Associate General Counsel, Patents & Technology
Title of authorized person signing

OCT 21 2005

- ☐ Recorded of assignment attached.
☐ Attached is a "STATEMENT UNDER 37 CFR 3.73(b)," establishing the right of the assignee to take action in this case.

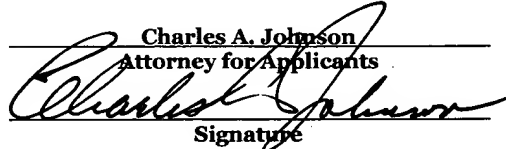
Respectfully submitted,



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CAJ/eav

I hereby certify that this correspondence is being deposited in the United States Postal Service as first class mail in an envelope addressed to: Attn: Certificate of Correction Branch, Commissioner for Patents, Alexandria, VA 22313-1450 on October 11, 2005.

Charles A. Johnson
Attorney for Applicants

Signature

October 11, 2005
Date of Signature

OCT 21 2005

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATION OF CORRECTION

PATENT NO : 6,950,816 *BI*
DATED : September 27, 2005
INVENTOR(S) : John M. Quernemoen and Mark G. Hazzard

It is certified that error appears in the above-identified patent and that said Letters Patent hereby corrected as shown below:

In the claims:

Claim number 3, Col. 17, line 12: following the term --includes-- the term --an--should be inserted.

MAILING ADDRESS OF SENDER:
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PATENT NO. 6,950,816

OCT 21 2005

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATION OF CORRECTION

PATENT NO : 6,950,816 **B!**
DATED : September 27, 2005
INVENTOR(S) : John M. Quernemoen and Mark G. Hazzard

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PATENT NO. 6,950,816

OCT 21 2005



Application No. 09/515,158
Amendment dated October 13, 2004
Reply to Office Action dated July 19, 2004

18 processor utilization limit and said determining and re-determining steps include determining
19 said hardware resources such that said desired percent processor utilization limit is maintained
20 and includes changing said number of processors required when necessary to remain within said
21 desired processor utilization limit.

1 2. (Canceled)

1 3. (Previously Presented) A method as recited in claim 1, the method further
2 comprising the steps of:
3 obtaining selected database requirements including an expected database size; and
4 determining the hardware resources needed for the yet-to-be built database management
5 system to satisfy the selected database requirements while remaining within the desired hardware
6 utilization limits.

1 4-9. (Canceled)

1 10. (Currently Amended) A method as recited in claim [[9]] 1, wherein said desired
2 percent processor utilization limit includes an upper [[an]] utilization limit to prevent over
3 utilization of said processors and said determining and re-determining steps include determining
4 said number of processors needed to keep below said upper utilization limit to prevent over
5 utilization of said processors.